Features
- Decommutator
  - Single channel serial data input
  - Accepts IRIG 106-96 serial data streams
  - FIFO based and RAM based architecture
  - Encodes data as an asynchronous embedded format
  - Uses empty flags to support data recovery (when operating in FIFO mode)
  - Accepts NRZ-L/RNRZ-L data and bit clock
  - RS-422, TTL or bit Synchronizer inputs

- PCM bit synchronizer
  - Bit rates up to 10 Mbps, NRZ codes
  - Data output into the host system PCM stream is limited by the bit rate setting of the host
  - Single-ended analog or RS-422 inputs
  - Analog input amplitudes from 0.1 to 5.0 Volts
  - Accepts all IRIG 106 codes as input
  - Provides NRZ-L output data with coherent clock
  - Includes clock sync indication

- Microsoft Windows application software included

Description
The DCM-101B is a bit synchronizer and decommutator board for use in TTC’s EDAU-20XX or CDAU-20XX series products.

The DCM-101B has a single channel bit synchronizer input that provides full featured clock reconstruction, data recovery and code conversion in a form factor compatible with TTC’s EDAU-2000 and CDAU-2000 product lines. Multiple boards can be placed within a single EDAU/CDAU host chassis. The board processes an analog PCM input or a differential RS-422 input at rates of up to 10 Mbps for NRZ codes and up to 5 Mbps for BiØ codes. The analog input impedance is programmable to 50Ω, 75Ω or 10kΩ and input amplitudes from 0.1 to 5.0 Volts are accepted. TTL and RS-422 compatible PCM data and 0° clock outputs are provided to drive cards requiring serial data and clock inputs.

The DCM-101B also has a single channel serial input decommutator. It operates in one of two modes, RAM mode or FIFO mode. The inputs can be sourced directly from the bit synchronizer or can be input directly to the decommutator in either single-ended TTL or differential RS-422 form.