THE DESIGN OF A HIGH-PERFORMANCE NETWORK TRANSCEIVER FOR iNET

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ABSTRACT

A critical element of the proposed iNET architecture is the development of a telemetry network that provides two-way communication between multiple nodes on both the ground and in the air. Conventional airborne telemetry is based on IRIG-106 Chapter 4 and provides only a serial streaming data path from the aircraft to the ground. The network-centric architecture of iNET requires not only a duplex communication link between the ground and the test article, but also a communication link that provides higher bandwidth performance, higher spectrum efficiency, and a transport environment that is capable of fully packetized Internet Protocol. This paper describes the development path followed by TTC in the implementation of its nXCVR-2000G, an OFDM 802-11a-based iNET-ready IP transceiver.

KEY WORDS

Ethernet, IEEE 1588, iNET, Transceiver, OFDM, IEEE 802.11a, IEEE 802.16

INTRODUCTION

The iNET program has reached its 5th year of operation and has recently shifted its focus from the definition of its network-centric telemetry architecture into the development of a set of standards that can be used to guide the production of hardware/software systems that can achieve this architecture. One of the key elements of the iNET architecture is the creation of an IP-based transceiver capable of enhancing traditional telemetry with wireless network connectivity. As part of the effort to advance the iNET standardization process, the Communications Link Standards Working Group has been formed to address the establishment and development of an open interoperability standard for a wireless network communication link for the aeronautical telemetry environment. The goal is to define a communications standard that is compliant with the existing published iNET architecture and provide the basis for a hardware specification allowing manufacturers to offer interoperable system component(s) on a competitive basis. The expectation is that the written standard will reside within IRIG-106 and will be matured in the same manner as the existing standards for serial streaming telemetry.

Teletronics Technology, Corp. is an active member of this standardization effort, in addition, we have begun our own development efforts to design and implement an iNET-compliant transceiver. The development effort serves two purposes; it provides the engineering personnel at TTC the ability to understand the real issues involved in creating a system that will meet the iNET requirements and, as such, allow us to provide meaningful feedback to the standardization process, and secondarily, it provides iNET the opportunity to have an actual implementation of a working iNET transceiver that can be used to solicit real-word feedback from actual customers.

This paper provides a high-level overview of the specifications of an iNET-compatible IP transceiver capable of satisfying the requirements defined for the communication link within the iNET architecture. In addition, a discussion of the architecture of the nXCVR-2000G, both from a hardware and software point of view, is provided.

INTRODUCTION TO THE nXCVR PRODUCT FAMILY

The goal of the nXCVR-2000G transceiver is to be compatible with the iNET communication standard. It is a Multi-Carrier (MC) IEEE 802.11a OFDM-based transceiver. The nXCVR family will offer a series of iNET–ready IP transceivers equipped with reconfigurable MC and Single Carrier (SC) modulations, as well as an enhanced wireless communication capability that will exceed the iNET standard for a wider range of potential customer needs. Figure 1 shows where the nXCVR transceiver family fits within the IEEE 802 wireless standards and the existing iNET specification.

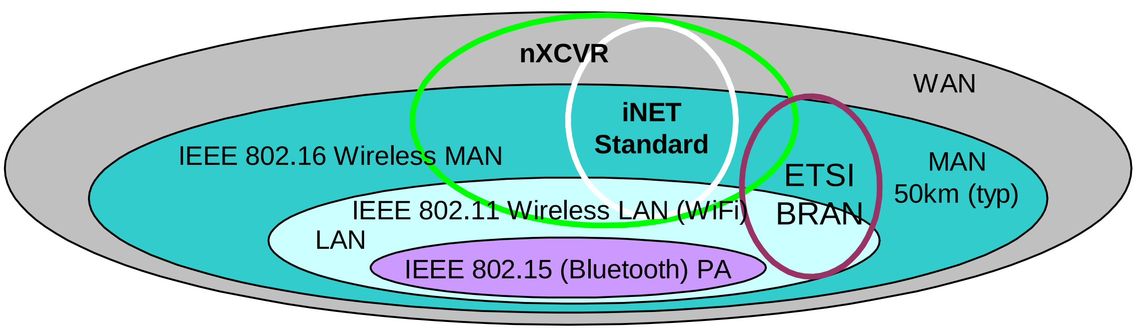

Figure 1: Overview of the nXCVR Transceiver Family in Relationship to Global Wireless Standards.

Through the use of a flexible and adaptive link quality control mechanism, the nXCVR will provide a high data throughput rate with superior multipath immunity and power efficiency. A brief list of its RF feature set is listed below. The specifications will be compatible with the forthcoming iNET standard, and many will exceed it.

- Multiple Frequency bands

- Data rate: 6Mbps to 54Mbps
- Default effective signal bandwidth: 16.25MHz
- Transmitter power 20W (typical) / 80W (max.)
- Reachable link distance of 50-200 nm
- Optimized for network-centric adaptive communications
    - Wide range adjustable OFDM bin effective BW: 625kHz ~ 16.25MHz
    - Wide range adjustable multipath immunity capability: min. 0.625 us to 20 us
    - Wide range adjustable power control
    - Wide range adjustable modulation waveform (MC, SC) scheme for optimum performance
    - Configurable strong Forward Error Correction Code (FEC): Convolutional code rate 1/2, 3/4, Reed-Solomon, LDPC AR4JA6144 rate 2/3
- Synchronization accuracy
- Multiple Modulation waveforms:
    - MC: OFDM (802.11a, 802.16) with BPSK, QPSK, 16QAM, 16PSK
    - SC: SOQPSK, PCM/FM
- iNET-compliant MAC protocol
- Interface: GPS Antenna, 10/100/1000 Ethernet, RS232, RS422, IMU, RF
- Physical dimensions: 3 W x 5 L x 3 H inches;
- Total power consumption: 100 Watts

A high-level functional block diagram of the nXCVR-2000G is shown in Figure 2 below.

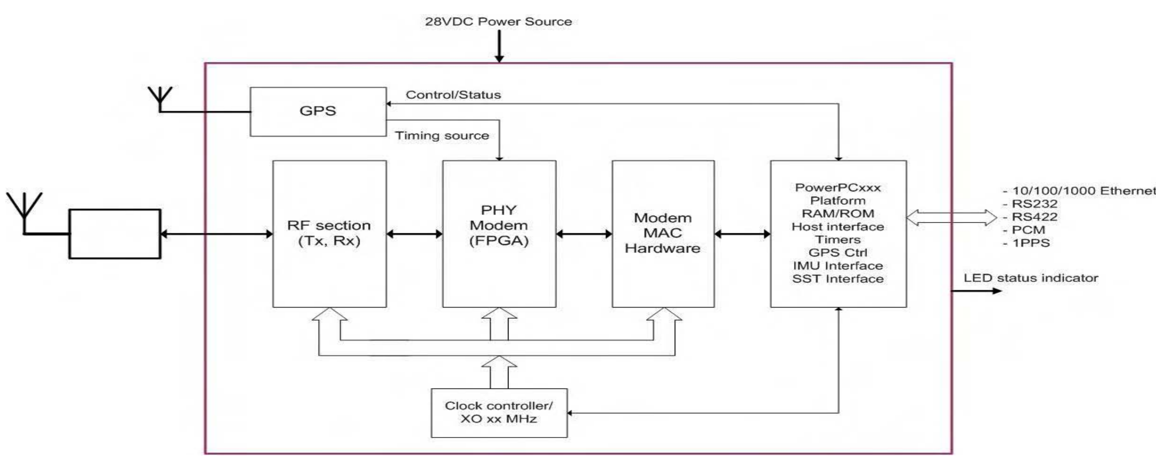

Figure 2: nXCVR-2000G Functional Diagram

We present a more detailed review of the nXCVR-2000G features and descriptions of its functional aspects in the following order.

- RF Transceiver section
- PHY digital modem section
- Microprocessor/IEEE-1588 subsystem section
- Software Architecture

RF TRANSCEIVER

Introduction

The implementation of OFDM within the iNET architecture introduces new challenges for the transmission media normally occupied by a traditional streaming FM transmitter and possibly a FSK uplink receiver. A TDMA structure that allows for the uplink and downlink to share the same RF spectrum drives up the power amplifier design complexity necessary to achieve a compliant OFDM waveform with typical current draw. The development of the RF transceiver for iNET is discussed in the following paragraphs.

Challenges

Some of the challenges for the traditional RF telemetry engineer to implement the program goals are as follows.

- Comply with the industry form factors associated with standard telemetry transmitters and receivers
- Consume the typical current draw for a 20 watt streaming transmitter
- Share RF subsections to the fullest extent to reduce size and cost
- Provide both TDMA and traditional waveform compatibility
- Provide variable input gain and output power to regulate the transceiver performance over the various flight test terrains that will be encountered
- Implement an agile system to accommodate varying bandwidth applications
- Considerations for loopback testing to support remote diagnostic capability

Exceeding the performance goals is critical to the performance of the overall link in the many environments that the Flight Test program will encounter. The form factor and dissipation are critical to provide a new system with backward mechanical compatibility. To assist in meeting this goal, the TDMA structure of the transmission media allows for sharing many of the RF front-end components, which that reduces the overall size and power consumption.

Various flight test scenarios and terrain must be supported by this solution. Due to the sensitivity of the modulation waveform and the TDMA structure to widespread multipath and link distances, a solution must provide an agile power/gain system to compensate for the effects of varying signal-to-noise ratios and distortions. True multilevel power/gain control has been determined to be a requirement for addressing these issues. This may include a varying bandwidth RF front-end and possibly antenna beam forming technologies to maximize the link margins to maintain the maximum data throughput.

With the networked nature of the system, remote access can be implemented and achieved to provide health status of the RF link with active adjustment of the system power/gain parameters to obtain optimal link performance at minimal power. Full loopback capability exists to support remote diagnosis of the various lines and RF links with this system, maximizing the system effectiveness for data validation and also enhancing the remote programming of each transceiver for center frequency and potential modulation types and indexes.

Architecture

The iNET Transceiver baseline is shown in Figure 3, consisting of the RF board assembly being controlled and operated from the FPGA board assembly and its external interfaces, e.g., Ethernet.

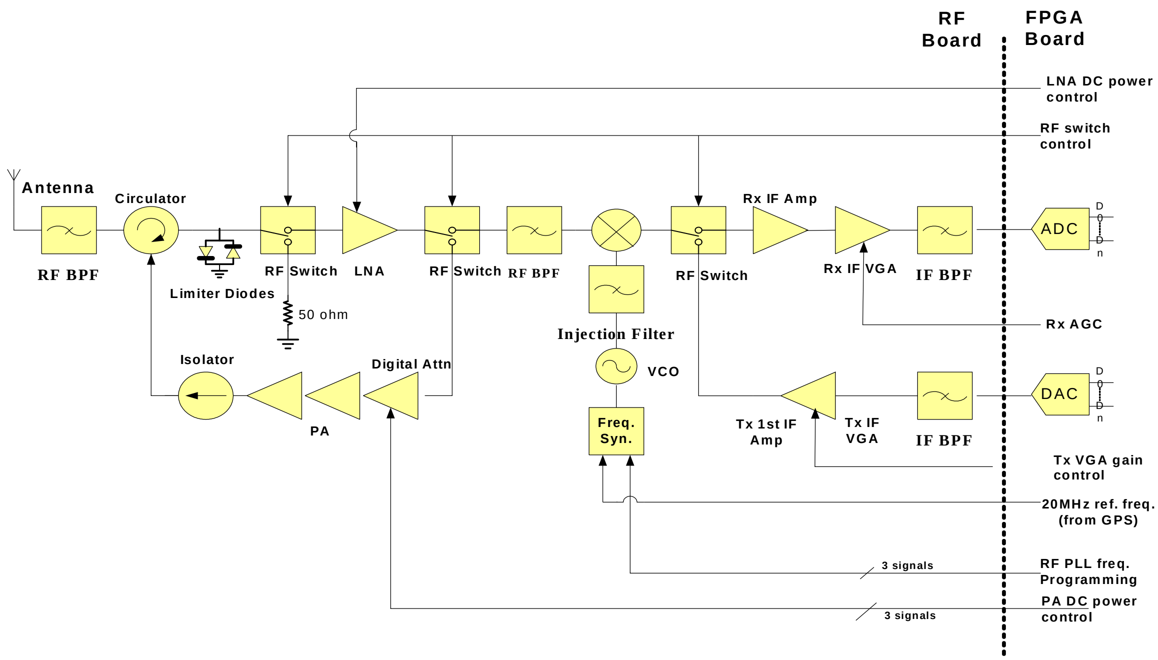

Figure 3: **iNET Transceiver Block Diagram**

Waveforms

The OFDM waveform generated is shown in Figure 4. The screenshot illustrates the spectrum from the resulting transmitter prototype that provided a 10W average, 125W peak pulse (PK-AVG is 11 dB), frequency at 2385 MHz with a 16.8 MHz bandwidth.

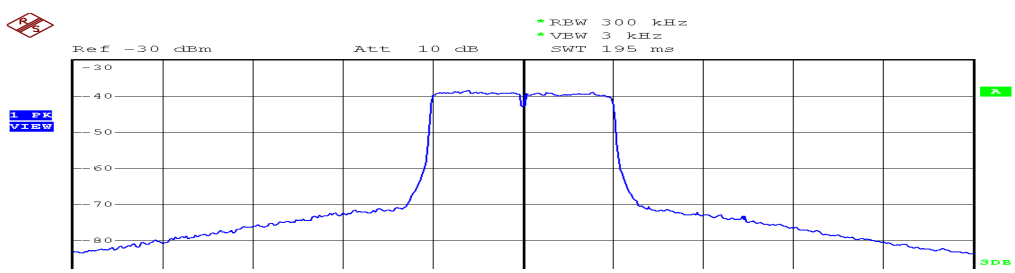

Figure 4: Prototype OFDM Spectrum

PHY DIGITAL MODEM: Modulation, Architecture & Description

The base-lined nXCVR-2000G employs an 802.11a-based OFDM modulation waveform. The top-level architecture of the PHY for Tx, and Rx is shown in Fig. 5 and Fig. 6, respectively.

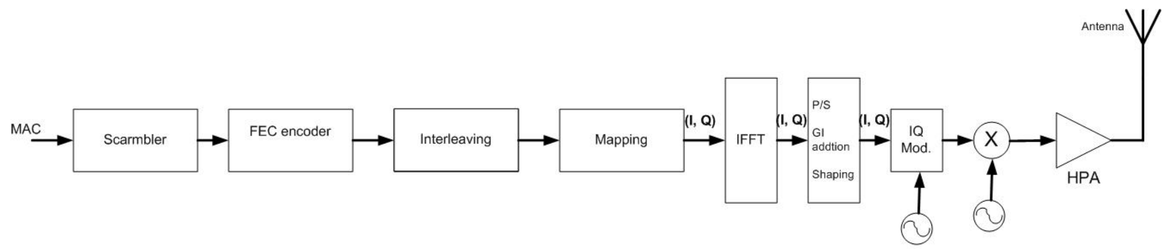

Figure 5: Functional View for the OFDM PHY (Transmit)

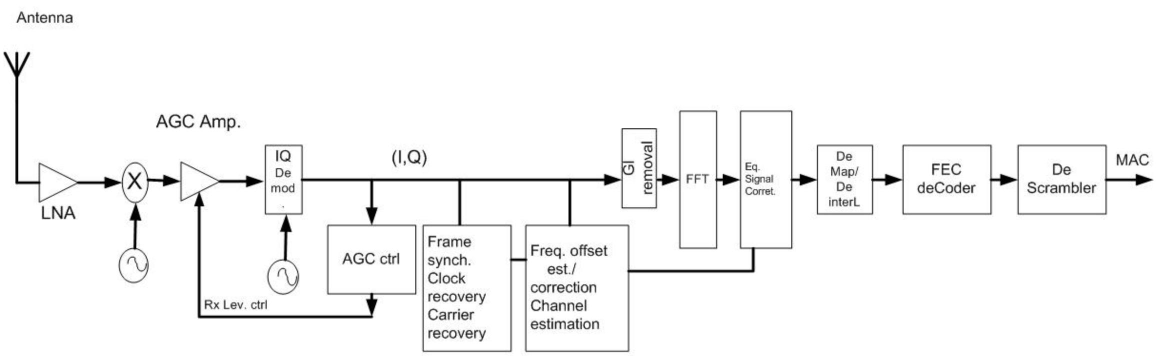

Figure 6: Functional View for the OFDM PHY (Receive)

Modulation, Data Rate and Forward Error Correction Code (FEC)

The nXCVR OFDM PHY is flexible and reconfigurable. Using the nXCVR modulation parameter control matrix, as shown in Table 1, it can be configured to any selected modulation-specific type and data rate from a wide range of modulation schemes suitable for different customer needs.

The modulation parameters include:

i) Modulation type:
   (a) Multi-Carrier (MC): OFDM BPSK, QPSK, 16QAM, 64QAM; SQPSK, CPM-FM;
   (b) Single Carrier (SC): SOQPSK, CPM-FM
ii) FEC type: iNET LDPC/AR4JA6144 code, 802.11a convolutional code, Reed-Solomon over GF(256) code
iii) FEC code rate:
   (a) 1/2, 3/4, 2/3 for 802.11a convolutional code
   (b) 2/3 for iNET LDPC/AR4JA6244 code
   (c) Variable rate, 188/204 as default for Reed-Solomon code (optional)

Modulation Parameter	Selectable Elements	Control bits
Modulation type	[MC{..},SC{..}]	4bits
FEC type, rate select	[AR4JA, Conv.{..}, RS{..}]	4bits

Table 1: Description of Modulation Parameter Control Matrix

The data rate is dependent on the modulation parameters {modulation type, FEC type, and FEC code rate}; Table 2 shows the available set of data rates provided by the nXCVR-2000G

	*Data rate; (Mbits/s)	*Code rate (R)	*FEC Overhead		**Data rate (Mbits/s)	**Code rate (R)	**FEC Overheard
BPSK	6	1/2	50%				
BPSK	9	3/4	25%				
QPSK	12	1/2	50%				
QPSK	18	3/4	25%		16	2/3	33%
16QAM	24	1/2	50%		32	2/3	33%
16PSK***	24	1/2	50%				
16QAM	36	3/4	25%				
16PSK***	36	3/4	25%				
64QAM	48	2/3	33%				
64QAM	54	3/4	25%				

*Using 802.11a specified FEC and code rate;
** Using iNET standard (draft) specified FEC and code rate;
***Using nXCVR-2000G extended modulation;

Table 2: Selectable Data Rates

FEC Performance employed in the nXCVR can be found from the iNET standard publication documents and IEEE publications.

MICROPROCESSOR/IEEE-1588 SUBSYSTEM

The nXCVR-2000G employs a microprocessor to control and manage its operation. The processor also interfaces to the IEEE-1588 logic to assist in the termination of the Precision Time Protocol (PTP). Figure 7 below shows a block diagram of the microprocessor and its associated support circuits.

The processor is responsible for executing the software that supports the operation of the transceiver, i.e., a real-time Linux operating system, IP stack, drivers, application software, etc.

To process the software in real-time, a high-performance processor is required. As such, the nXCVR uses a RISC-based processor with a core that runs at 800 MHz. This translates to a peak performance of 1600 Dhrystone 2.1 MIPS (DMIPS). To help keep the processing core's pipelines full, a high bandwidth memory interface in used. Connected to the memory bus is 256 Mbytes of Double Data Rate (DDR) Synchronous Dynamic RAM (SDRAM). At a width of 64-bits and a bus speed of 133 MHz, the memory interface has a peak bandwidth of 2.1 GBps. The system software is stored in non-volatile memory (flash memory) that is connected to the processor's Local Bus.

The processor is also an important part of the nXCVR network interface. The processor contains the Media Access Control (MAC) logic needed to interface with the wired IP network. Specifically, a gigabit MAC is used to implement a gigabit Ethernet (GbE) interface. This interface has two important roles. The first is to provide the primary data path to and from the test article's on-board IP network. The second is to provide an interface to the IEEE-1588 PTP. In Figure 7, the processor's GbE MAC is connected to a FPGA via a Reduced Gigabit Media Independent Interface (RGMII) Bus. A second RGMII Bus is then connected to a GbE PHY device that interfaces to the physical GbE port. The FPGA includes the necessary logic to terminate the PTP.

To enable the nXCVR to perform the duties of a network-timing source, a GPS receiver is included. The processor controls the GPS receiver using one of its UARTs. The function of the receiver is to lock to a GPS source and provide a timing reference to the PTP logic. The PTP logic uses the reference to generate timing to the rest of the test article's network, via the GbE interface, and to the wireless interface. In this way, the nXCVR can perform the duties of an IEEE-1588 Grand Master Clock.

In addition to the functions mentioned above, the processor uses a second MAC to interface to a second Ethernet PHY device. The second Ethernet port can be used for network management purposes, health and statistics monitoring, software upgrade, etc. A serial communications interface is also provided for debugging purposes.

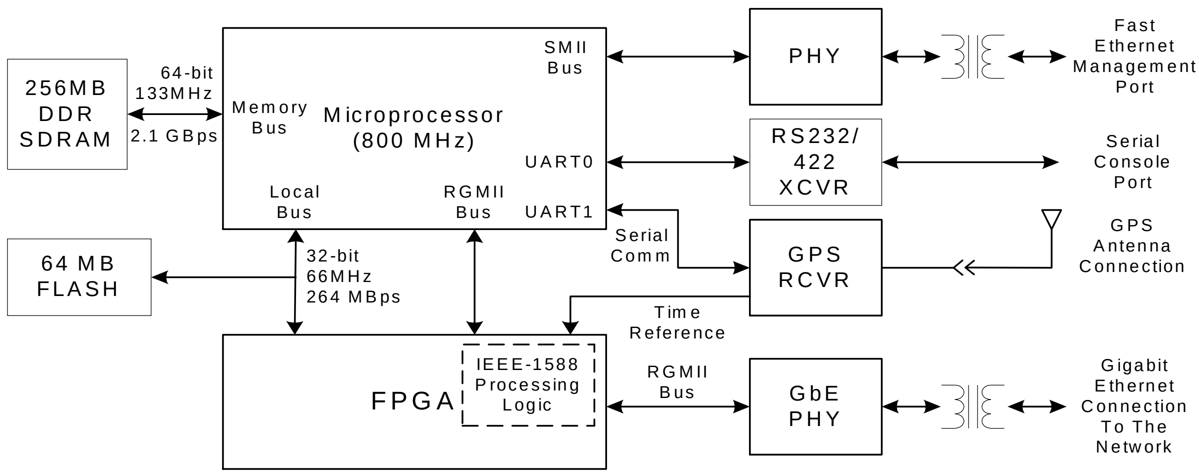

Figure 7: Microprocessor/IEEE-1588 Block Diagram

SOFTWARE ARCHITECTURE

The software architecture of the iNET transceiver is organized into 4 layers: application, kernel, driver, and hardware. The functions needed to implement the communication link have been distributed between these four layers in a manner that provides the best way for Teletronics to achieve its implementation goals:

1) Short time to market – the software architecture is designed to allow for as much software reuse as possible from existing Teletronics network products.
2) Flexibility – the iNET communications standard is still relatively immature, and many decisions regarding technology and standards are unresolved. The bulk of the Media Access Protocol will be implemented within the application layer to allow for ease of field upgrades.
3) Performance – While much of the MAC layer is implemented in software, critical functions will be assigned to the FPGA implementation to allow for satisfying the timing requirements needed to implement the TDMA-based packet processing.

An overall view of the software architecture from a logical viewpoint is show in Figure 8.

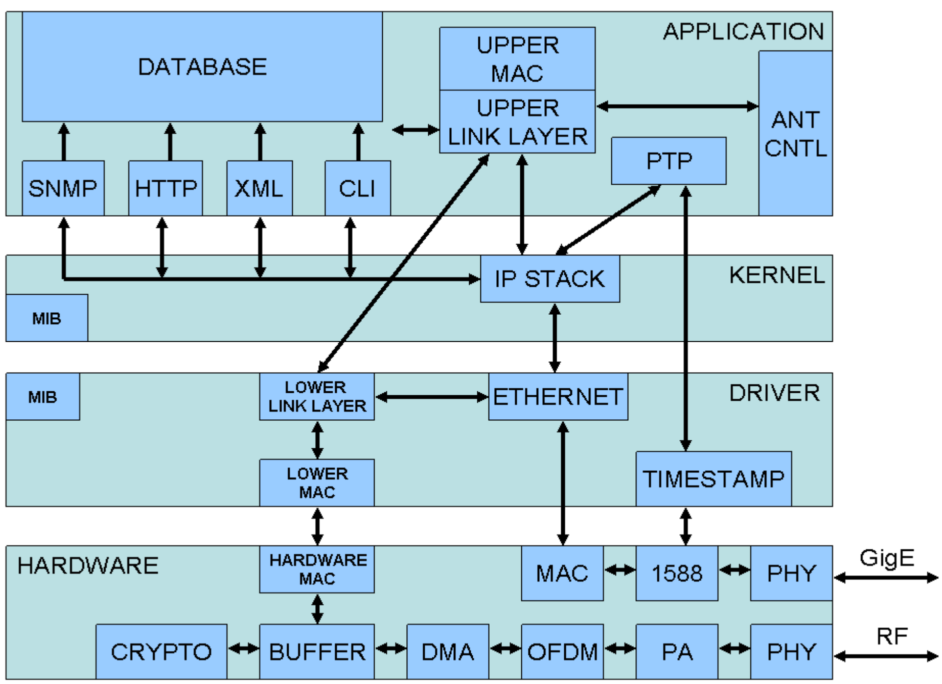

Figure 8: Logical Software Architecture

Configuration, Control, and Management operations occur within the application layer. The Database provides the centralized mechanism for maintaining the parameters used by these operations. Both standard and custom MIBs will be implemented within the kernel layer (such as the IP stack) and within drivers (the iNET link layer) for access via the SNMP interface thru the database. Non-volatile parameters are read and/or written directly to the database, whereas volatile parameters pass through the database and reference the affected component directly. SNMP is used primarily for access to statistics and asynchronous event notifications. The XML interface and its associated schema provide a static configuration interface to the device. Both the HTTP and CLI (command line interface) interfaces are designed to provide a dynamic means of reading and writing the device parameters.

A key decision in the design of the iNET MAC is the partitioning of its functions within the software and hardware layers in the device. For maximum performance and minimal flexibility (usually possible for an established standard), the MAC and PHY are usually implemented as a hardware element. To maintain maximum flexibility for iNET, Teletronics has chosen to split the MAC into five implementation blocks, four in software and one in hardware (FPGA). The role of each functional block is described below.

1) Upper MAC
    a. User Management
    b. User Configuration
    c. QOS Policies
    d. OFDM Configuration
2) Upper Link Layer
    a. Hub/Neighbor Discovery
    b. Authentication
    c. Authorization
    d. RF Link Parameters
3) Lower Link Layer
    a. Link Construction
    b. Link Deconstruction
    c. Link Recovery
4) Lower MAC
    a. QOS Implementation
    b. Error detection and Retransmission
    c. Packet Framing
5) Hardware MAC
    a. Epoch Synchronization
    b. Timeslot Synchronization
    c. Data Movement
    d. Encryption

The iNET transceiver will support a hardware-assisted 1588 implementation. The PTP protocol stack will reside in the application layer and interface with both the IP stack for UDP packets and with the timestamp driver for timestamps taken from the 1588 hardware which partitions the Ethernet MAC and the Gigabit Ethernet PHY. The reference clock from the 1558 hardware is used to synchronize the MAC/PHY with other communication nodes.

REFERENCES

[1] Cheng Y. Lu, Yimin Zhang, Jinsong Wu, Paul Cook, Xin Li, and Moeness Amin, *Antenna Array Beam-Forming Technology: Enabling Superior Aeronautical Communication Link Performance*, Teletronics Technology Corp., Newtown, PA 18940 & Center for Advanced Communications, Villanova University, Villanova, PA 19085, Proceedings of the International Telemetering Conference (ITC 2008), San Diego, CA USA, October 27-30, 2008.