

# UTILIZATION OF AN IEEE 1588 TIMING REFERENCE SOURCE IN THE iNET RF TRANSCEIVER

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## ABSTRACT

Synchronization of the iNET communication link is essential for implementing the TDMA channel access control functions within the transceiver MAC transport layer, and providing coherent signal demodulation timing at the transceiver PHY layer. In the following implementation, the 1588 timing reference source is the GPS receiver. Because it is being used in the Ground Station Segment and Test Article Segment, it becomes feasible to utilize the 1588 timing reference for cross-layer (MAC+PHY) iNET transceiver synchronization. In this paper, we propose an unified iNET transceiver synchronization architecture to improve iNET transceiver performance. The results of the synchronization performance analysis are given.

**Keywords:** *Ethernet, 1588, cross-layer synchronization, GPS, OFDM*

## INTRODUCTION

The architecture of the iNET (Integrated Network-based Telemetry) communication link critically relies on synchronization of time within the distributed network. Its importance resides in the synchronized nature of iNET RF transceiver TDMA (Time Division Multiple Access) MAC (Media Access Control) protocol scheme and within the use of OFDM (Orthogonal Frequency-division Multiplexing) as the PHY modulation waveform. The absolute accuracy of the timing synchronization between individual transceivers will improve or degrade the quality of network application services such as communication scheduling, sensor data timestamps, as well as network formation between nodes and overall network throughput efficiency.

The issues specific to time synchronization concern timing issues from the physical-layer (PHY), digital signal processing (DSP), and application-layer scheduling. In this paper, we will focus on the synchronization of the iNET RF transceiver MAC layer and the

OFDM-based PHY layer. A set of algorithms is presented which provide a system level GPS-based timing synchronization scheme for the transceiver. The timing requirements of the system are derived from the needs of the MAC layer and the PHY layer. The MAC layer timing requirements refer to synchronizing the TDMA epoch period between multiple transceivers and the determination of the individual timeslots and their adjustment. The PHY layer timing model requires estimating the OFDM signal frame boundary (Frame Synchronization), performing symbol clock estimation and/or correction, determining carrier frequency and providing phase estimations and correction.

## OFDM TIMING CONSIDERATIONS

Figure 1 below shows a simplified baseband model of an OFDM modulation system. On the transmitter side as shown in Fig. 1, the core DSP operations are an Inverse Fourier Transform (IFFT) operation and a time-domain Guard Interval (GI) insertion operation. On the receiver side, based on the availability of a timeslot as determined by the MAC TDMA channel access control scheme, and with proper synchronization, the reverse operation of the transmitter will be executed.

There is a fundamental distinction between a Single Carrier (SC) modulation waveform such as Shaped Offset Quadrature Phase-Shift Keying (SOQPSK) and a Multiple Carrier (MC) such as OFDM. In an OFDM modulation scheme, the user data is directly modulated by signal frequency in amplitude and phase as opposed to SOQPSK, where the user data is directly modulated by the time domain waveform. This fundamental distinction imposes unique timing synchronization issues. A detailed discussion on this distinction is presented in this paper.

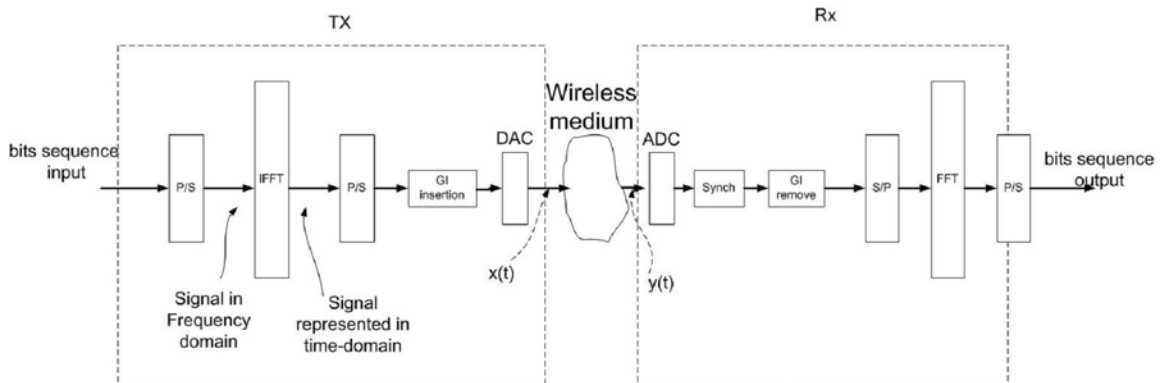


Figure 1: Simple model of OFDM-based transmission system

## SYNCHRONIZATION CHALLENGES

The in-progress iNET communication link standard has specified the OFDM IFFT default size as  $N = 64$ . The input bit sequence to the PHY transmitter is being assigned to 48 out of the 64 bins from the IFFT with a predefined bits-to-IQ signal mapping (e.g. 2 bits to QPSK). This bit mapping is performed at each IFFT bin. The rest of the 16 bins are set to zero. Through the IFFT operation, the user data bit sequence is transformed into a time domain signal. As shown in Fig. 1 the transmitted signal passes through a wireless communication medium to the receiver node. Because of this, the signal at the receiver input may be degraded with phase and amplitude distortion. A signal clock timing error (phase and frequency) at the receiver end may be introduced due to the wireless propagation of the RF waveform and the timing inaccuracy of the local oscillator at the receiver end. The synchronization module in the receiver has to be properly designed to accurately recover the signal's timing, carrier frequency and phase.

In general, assuming a perfect local oscillator reference source is available; the source of synchronization timing errors between transceiver nodes consists of [1]:

- (1) Send time  $\text{delt\_T1}$ : This is the time spent in the MAC layer for constructing the message being sent. It also includes the overhead of any operations need in the MAC link-layer processing.
- (2) Access time  $\text{delt\_T2}$ : This is the time spent in the PHY/MAC layer. It accounts for the time delay waiting for a channel to be available for transmission.
- (3) Propagation time  $\text{delt\_T3}$ : This is the time spent by the signal traveling in the transmission medium from the transmitter to the receiver.
- (4) Receive time  $\text{delt\_T4}$ : This is the time spent in the receiver PHY and MAC to transfer the message to the host.

(1) and (4) are implementation dependent issues that are not the focus in this paper. The primary concern is with the synchronization timing error sources (2) and (3), as well as the impact of a non-ideal local oscillator used by the transceiver which introduces a timing error during signal synchronization. As shown, the synchronization timing error comes from both the MAC and PHY layer. Any timing synchronization algorithm must be a cross-layer joined process in order to provide an effective solution.

## iNET RF TRANSCEIVER TIMING SYNCHRONIZATION ERROR ANALYSIS

The primary advantage of OFDM over a single carrier (SC) modulation waveform, e.g. xQPSK, is in its superior capability to handle severe channel conditions, narrowband interference, and frequency-selective fading (multipath, micro-reflection, etc.) due to its simplicity of frequency domain equalization operations and channel estimation. However, besides other known issues such as high peak-to-average power ratio, the OFDM modulation waveform is sensitive to the inaccuracy of timing estimation. This

issue can be illustrated by examining the properties of the core operations during OFDM modulation.

A frequency domain signal  $X(f)$  is defined as the Fourier Transform of a time domain signal  $x(t)$ , i.e.

$$X(f) = \text{FFT}\{ x(t) \}; \quad (1)$$

From the properties of a Fourier transform[2], it can be shown any timing estimation error in signal  $x(t)$  will result in its corresponding frequency domain signal  $X(f)$  being modulated by a corresponding phase.

$$x(t - \tau) \leftrightarrow X(f) \exp(-j 2 \pi \tau f) \quad (2)$$

Eq. (2) implies for given frequency the OFDM signal will suffer from a rotation of  $(2 \pi \tau f)$  degrees in the I-Q constellation plane. Fig. 2 and Fig. 3 show the given timing error  $\tau = 24.2\text{ns}$  of the OFDM signal I-Q constellation with and without timing estimation error compensation.

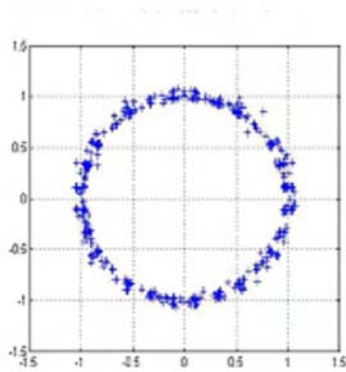


Fig. 2 OFDM I-Q constellation w/o timing estimation error compensation

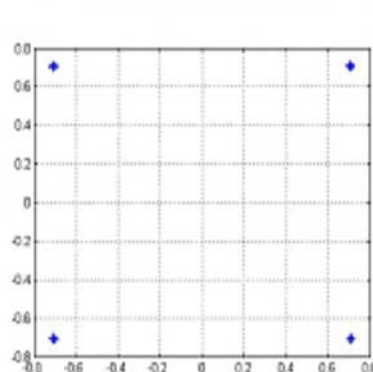


Fig.3 OFDM I-Q constellation with timing error compensation

In wireless transmissions, the received signal timing estimation error is due to nondeterministic nature of the timing reference source and signal propagation time. Fig. 2 shows the OFDM signal I-Q constellation with a timing estimation error of 24.2 ns. The phase error in the I-Q constellation is determined by eq. (2). This timing error will directly cause burst errors in the data. Fig. 3 shows, with receiver timing estimation error compensation, the received signal I-Q constellation can be stabilized and therefore, no data errors occur.

Comments:

- (1) The deterministic timing error, as shown in Fig. 4, when the timing reference estimation error of the received signal is in order of nanoseconds, that the EVM penalty will be on order of greater than 5%

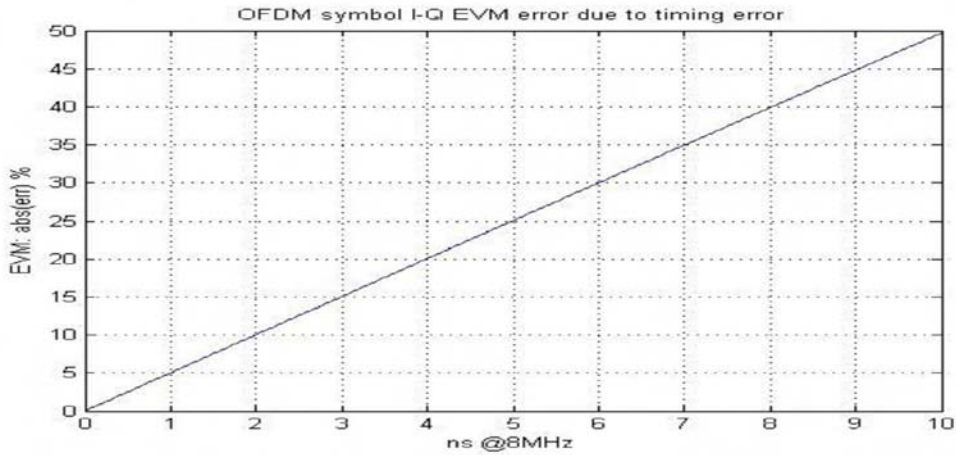


Fig. 4 OFDM EVM error due to timing error

- (2) The random timing estimation error: The clock jitter in a local oscillator will introduce a nondeterministic random uncorrelated phase noise in the OFDM I-Q constellation. The equation (2), as well as Fig. 4, is valid as the first-order estimation of the EVM error due to random clock jitter. A more precise estimation can be obtained by simulation. Fig. 5 shows OFDM I-Q constellation with a clock jitter EVM penalty of 8%;

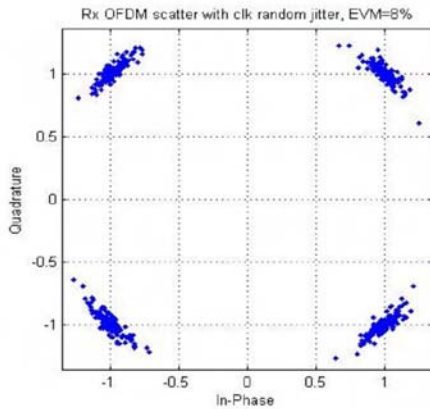


Fig. 5: Rx OFDM I/Q with clock jitter

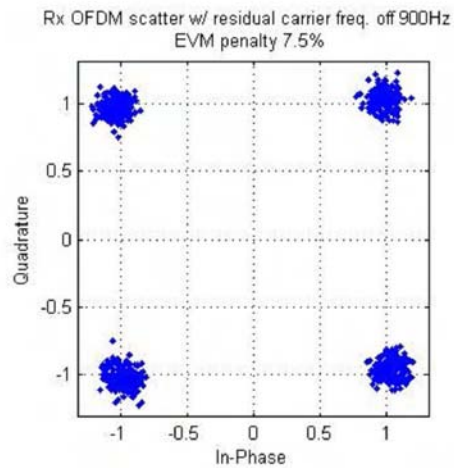


Fig. 6: OFDM I/Q, with residual frequency offset

- (3) Due to the local oscillator frequency instability, the carrier frequency in the received signal may not be able to be fully removed. This frequency inaccuracy will be translated as inter-symbol interference in the OFDM I-Q plane and will increase the EVM error penalty as shown in Fig. 6. Theoretical analysis can be easily derived using Eq. (1), Eq. (2), and the duality property of the Fourier transform. Details can be found in ref. [2].

## **CROSS-LAYER TIMING SYNCHRONIZATION**

The iNET communication link protocol has specified TDMA as its MAC link-layer access protocol. The use of TDMA requires a common clocking signal within the system, either through the use of a global clocking source or a clock recovery algorithm. While it's common in point-to-point communication channels to use clock recovery as a means to synchronize data flow between the two systems, in the case of iNET, the environmental challenges and the sensitivity of OFDM to clocking errors will make achieving a reliable, high bandwidth communication channel difficult. Normally, in the case of geographically distributed communication nodes, there isn't any availability of a highly synchronized clock. However, in the case of iNET, the test article will depend upon the availability of 1588 to distribute a common clock source over the local acquisition network for timestamp synchronization. Because of the inherent requirement for a highly accurate network clock in the iNET architecture, it makes sense to consider making use of 1588 timing as the node to node global timing reference. Current 1588 network timing synchronization technology with a GPS global timing reference source can achieve nanoseconds jitter using clocks with 1 to 2 PPM instability. These performance constraints suggest that the clock reference can not only be used for the MAC layer for TDMA timeslot configuration, but also can be used as the PHY layer coherent signal demodulation timing reference. In the proposed implementation, the 1588 timing reference source is a GPS receiver; and because it is being used in both the Ground Station Segment and Test Article Segment, it becomes feasible to utilize the 1588 timing reference for cross-layer (MAC+PHY) iNET transceiver synchronization.

## **GPS CLOCK SYNCHRONIZATION**

The first basic question to examine is to determine how accurately physically separate network clocks can be synchronized. To test this situation, the following experiment was conducted. Two independent GPS antennas were connected to 4 different GPS receivers. Three of the receivers were 1588 switches, and one was an independent GPS receiver. The 1PPS from all 4 devices were attached to an oscilloscope, using the independent GPS receiver's 1PPS output as the signal trigger. The oscilloscope was configured for histogram persistence, and the configuration was left to operate for 24 hours.

The resulting output is show below:

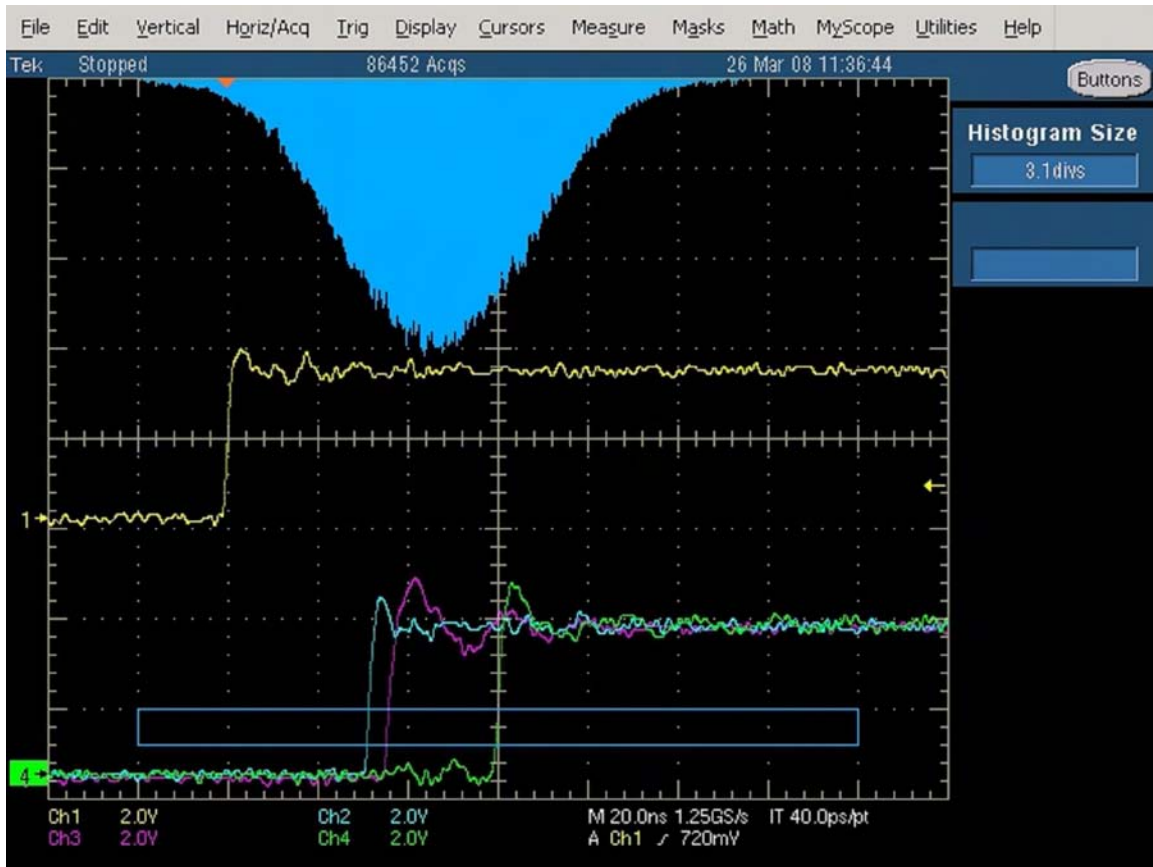


Fig 7: GPS-based 1PPS Synchronization

The yellow trace in the middle represents the baseline GPS receiver's 1PPS output. The blue, green, and violet traces at the bottom represent the 1PPS outputs of the 3 1588 switches. Each hash mark on the center line represents 4 nanoseconds. The inverted bell curve as the top represents the average position of the switches' 3 1PPS outputs over 86,452 seconds. There is a constant offset between the baseline GPS and the 3 switches, but for the purposes of this experiment, it can be ignored. From the width of the bell curve, the variance (and therefore, the jitter) can be calculated for the 3 switches; each one generating its own 1588 clock source based on the clock derived from its GPS receiver. The absolute spread is  $\pm 68$  nanoseconds, and the 95% level is  $\pm 49$  nanoseconds.

## TDMA SYNCHRONIZATION

Time-Division Multiple Access (TDMA) is a digital transmission scheme that allows a number of users to access a single radio-frequency channel without interference by allocating unique time slots to each transmitter within the channel. iNET has specified the use of TDMA as the mechanism to share bandwidth between the ground station and

multiple airborne test vehicles. This is accomplished by introducing the concept of an epoch, which corresponds to a sequence of repeating timeslot assignments for all nodes of the network. Epochs might range from 10 to 1000 milliseconds and the timeslots are defined by their non-overlapping starting and stopping times within the epoch. Between timeslots, guard bands are allocated to account for timing inaccuracies and propagation delays that will exist in a real-world system. Within a single timeslot, one or more OFDM frames could be transmitted, each with their own guard bands. An illustration of a typical iNET communication epoch is shown below:

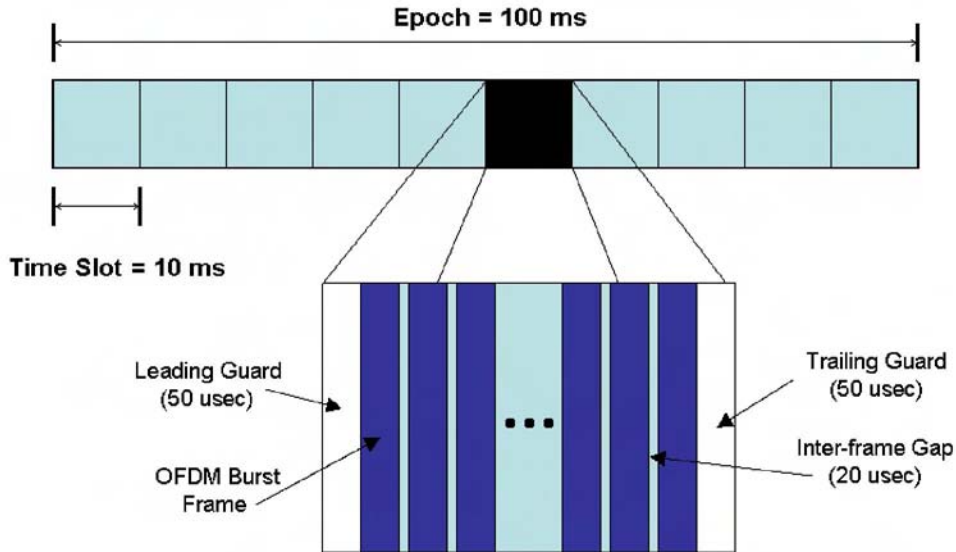


Fig 8: Typical iNET Epoch configuration

The 1588-derived clock would form the timing reference used by the transceivers to mark epoch and timeslot periods and synchronize the transmission and reception of OFDM burst frames between different transceivers. The allocation of timeslots to transceivers could be done either statically or dynamically and would be based on quality of service (QOS) and/or bandwidth requirements. Given an inherent synchronization inaccuracy of  $\pm 50$  nanoseconds, one could safely use a 1 microsecond resolution interval in the timeslot definitions and synchronize multiple transceivers to the same TDMA epoch and timeslot definition accurately.

### OFDM SYNCHRONIZATION

Synchronization within the OFDM modem requires that the jitter present in any 1588 derived clocks must be minimized. As illustrated within figures 2 and 3, timing error compensation can recover the OFDM burst frame information in the presence of clock skew, but any clock jitter will quickly degrade the ability of the modem to discern individual OFDM symbols from the input signal. The 1588 algorithm works by generating its own internal clock reference and comparing its own absolute time with

time communicated to it by the 1588 time grandmaster. Differences between the local clock and the master clock translate into clock adjustments that are applied to the local clock to zero out the local drift influences. These clock adjustments translate into clock noise as seen by the OFDM modem and degrade the signal to noise ratio during data recovery. In order to minimize this effect on the OFDM modem, careful measures need to be taken to smooth out this jitter as seen by the modem without compromising the ability of the 1588 clock to smoothly and accurately track drift between itself and the system master clock. There are many ways this can be accomplished; the diagram below describes one approach to minimize the 1588 clock noise as seen by the OFDM modem.

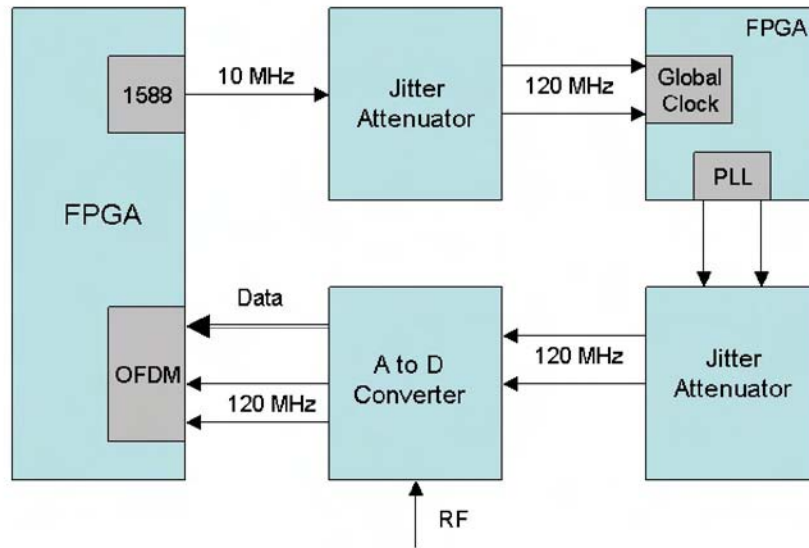


Fig 9: 1588 Clock Jitter Attenuation

The 1588 logic within the system generates a 10 MHz clock that is adjusted to smoothly track the network master clock. This clock is fed into a jitter attenuator which translates this clock into a differential 120 MHz clock. This clock is then routed back into the FPGA as a global input clock and re-synthesized using an internal PLL. This new clock is then output from the FPGA and fed into a second jitter attenuator. The output of the second jitter attenuator is used to clock the analog to digital converter which provides raw RF digital data to the FPGA used to implement the OFDM modem. The use of the two jitter attenuators and the conversion of the original clock into a PLL synthesized clock allows the system to reduce the 1588-induced jitter to a level sufficient to provide a stable clock that can be used to synchronize the OFDM modem to the input RF signal.

## CONCLUSION

Synchronization of the INET communication link through use of a 1588-derived clock source allows for the construction of a very general purpose transceiver. The ability to make use of a globally available clock source which can be used to locally synthesize

reference signals that control both the TDMA needs and OFDM modem needs to the iNET transceiver will help to resolve two difficult obstacles to the construction of a practical system. This paper has presented some the issues regarding the impact of clock jitter on OFDM signal recovery and the usefulness of applying 1588 clock synchronization technology to the problem of TDMA and modem synchronization.

## **REFERENCES**

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- [2] A Paupolis, *The Fourier Integral and its Applications*, New York; McGraw-Hill, 1962