

Design of a Gigabit Distributed Data Multiplexer and Recorder System

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Abstract

Historically, instrumentation analog tape based data recorders did not have a built-in data multiplexer, due to the nature of multiple track capability. Digital tape based recorders have been available with and without built-in data multiplexers. Recent solid-state data recorders, and in particular, the high capacity and the high data rate systems, have been assumed to include the solid-state media and multiplexer electronics within a single unit.

This paper challenges the assumption of a single multiplexer/solid-state unit when a large amount of data and large number of input sources are to be recorded. This paper describes a distributed data multiplexer and recording system, acquiring data from high-speed avionics data busses (Optical Fibre Channel and 1394B), PCM, wideband analog, video, and others. In addition, each multiplexer within the distributed system operates as a data acquisition unit for data retrieval down to the parameter level from input channels for transmission of flight safety information.

Key Words

Multiplexer, Recorder, Gigabit, Data Acquisition, Solid State

Introduction

Instrumentation engineers are in a constant struggle to accommodate ever-increasing demands to acquire and record a wide range of input sources from low data rates to very high (gigabit) rates. These data sources may include PCM, video, 1553 bus data at the low to medium rate, and Ethernet, FireWire, Fibre Channel, and other packetized digital communication at the medium to very high data rates. The variety and rates of data sources dictates that the multiplexer/recorder system must utilize high power wide bandwidth processor/bus architecture solution. Such a solution provides a designer with the choice of a very-high rate multiplexer at a cost of minimal I/O slots. In addition, some newer avionics data busses such as FireWire and Fibre Channel must be acquired as close as possible to the multiplexer/recorder unit.

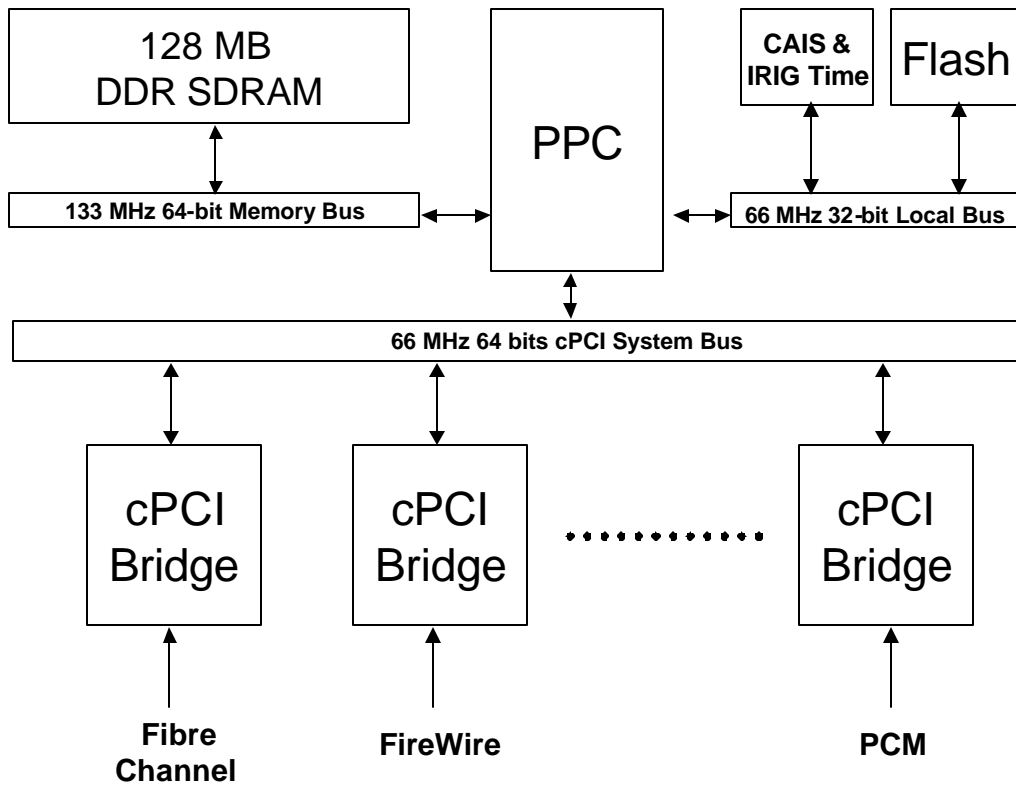
The paper will describe a multiplexer architecture that provides the user with the flexibility to multiplex large amount of data sources with low to very high data rate, and the ability to locate the unit as near as possible to the data sources, using a distributed data multiplexer solution. This layered system approach allows the flight test engineer to apply a multiplexer/recorder system in natural and incremental steps to accommodate upwards of gigabit data sources in an evolutionary manner.

Multiplexer / Recorder Architecture

An extensive and exhaustive evaluation was made in the development architecture of the multiplexer system shown in Figure 1. There are four core functions that together make up the multiplexer architecture that include:

- ? Backplane
- ? Processor
- ? Operating system
- ? Acquisition I/O cards

Figure 1 Multiplexer System Architecture



Backplane: A CompactPCI Bus-like backplane was chosen as the backbone of the unit. The backplane operates with 64-bit wide at 66 MHz operating rate using up to four I/O slots. This translates to a peak bandwidth of 528 megabytes per second (MB/s). Accounting for protocol overhead, bandwidth of over 200 MB/s is realizable within the multiplexer. Several signals were added to the backplane bus to meet IRIG-106 Chapter 10 time tag requirements, and other miscellaneous signals.

The design allows a migration path to higher bandwidth using the PCI-X protocol at the expense of fewer slots. The PCI-X provides a more efficient protocol that can result in a peak bandwidth exceeding 1 GB/s. The backplane can operate with 33 MHz rate in order

to increase the number of I/O slots to six. This translates to a peak bandwidth of 264 MB/s.

Processor: The multiplexer's backplane bus is controlled and managed by an overhead card with a PowerPC core processor. The processor and its peripherals form the basic building block upon which the unit architecture is based. The PowerPC core includes a PCI-X Bus controller, DDR-SDRAM controller, a peripheral bus controller, two Fast Ethernet MACs, two UARTs, two I2C Bus controllers, and other functions. The processor core has a peak performance rating of 800 Dhrystone 2.1 MIPS. Peak performance is attained with the help of integrated Level 1 instruction and data caches. Another key element to the performance is the memory controller. A high performance Double Data Rate Synchronous Dynamic RAM (DDR-SDRAM) controller, which is capable of peak data rates of 2.1 gigabytes per second, is supported. Adding to the primary functional blocks of the processor is a PCI-X Bus controller. The controller supports both 64-bit conventional PCI and PCI-X Bus protocols. At a maximum speed of 133 MHz and in PCI-X mode, the bus has a peak data rate of just over 1 gigabyte per second. In conventional PCI Bus mode, the peak data rate is 533 megabytes per second. Another important interface to the processor is the peripheral bus. The available 32-bit demultiplexed, general-purpose bus is ideal for interfacing to non-volatile memory, SRAM and slower peripheral devices. The peripheral bus can operate up to 66 MHz for a peak rate of 266 megabytes per second.

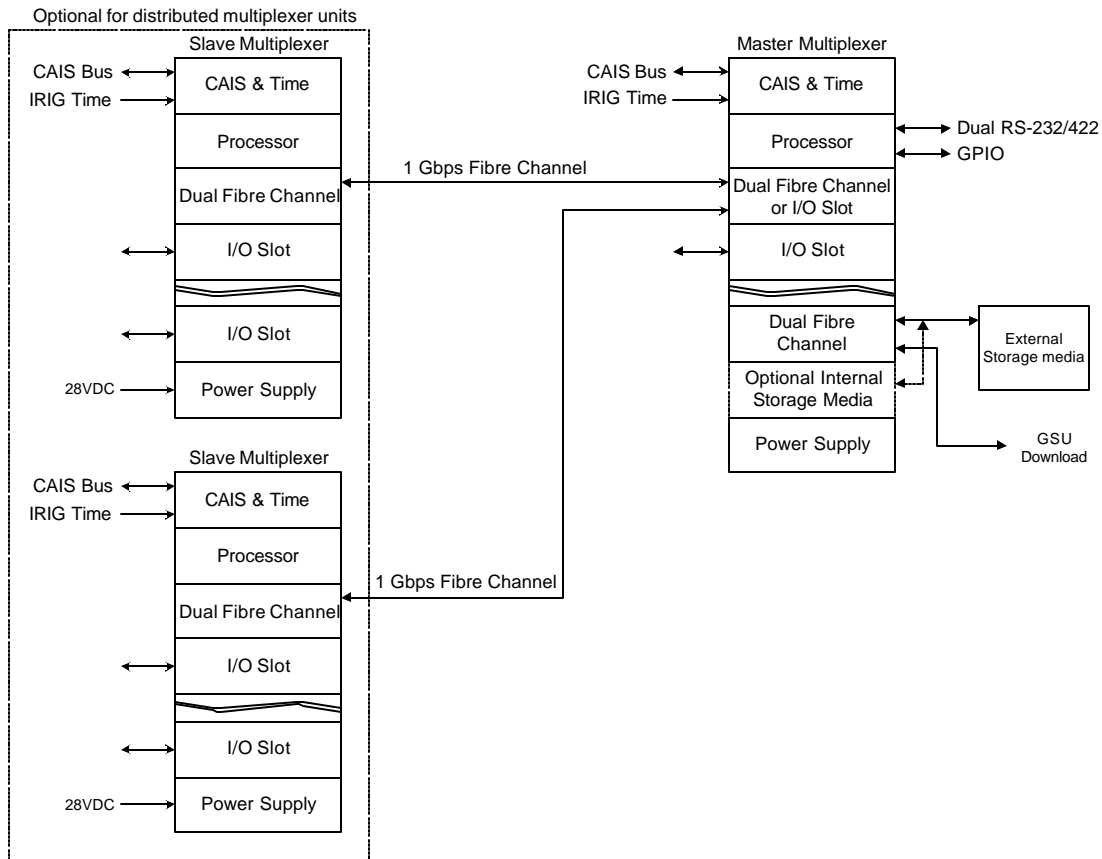
Operating System: The operating system used is a customized 2.4.18 Linux distribution that provided a preemptive kernel with real time scheduling. It provides a very good support of the processor, FireWire, and Fibre Channel. Development cost, runtime cost, source code, IDE tools, and real-time capability are all-important factors in the use of the operating system of the multiplexer.

Acquisition I/O Cards : The architecture allows the interface with peripheral I/O cards via the PCI bus. Each I/O card contains either a PCI2.2 or PCI-X 1.0 compatible bridge. The bandwidth requirement depends upon the type of peripheral card used. The type of cards range from low to medium bandwidth such as 1553 bus, PCM, video, etc., and the medium to very high bandwidth cards such as FireWire, Ethernet, Fibre Channel, etc.

Distributed Multiplexer Architecture

A multiplexer unit is limited in the number of peripheral I/O slots due to the high-speed nature of the backplane. In addition, the physical distance between the data source (i.e. FireWire) and the multiplexer must be such that no violation will result in the source's cable length. A distributed (or multiple box) multiplexer system overcomes both issues, and provides an elegant system solution. This architecture uses a multi-slot chassis populated with a common set of system and peripheral cards and interconnected into a group of 1-5 units for integration into a total onboard flight multiplexer / recorder package. An example of configuration is shown in Figure 2.

Figure 2 Integrated Multiplexer/Recorder Package



The external storage media is connected to the master multiplexer through a fibre channel interface. Slave multiplexers communicate with the master unit through a dedicated point-to-point fibre channel cable operating at 1 Gbps. Unit configuration of master vs. slave is done through a software load. Each unit in the distributed system contains a fixed number of slots and the number of slots is dependent upon the required backplane speed. It is assumed that the designated master unit will operate at an equal or higher speed than the slave units. The baseline unit supports a total of 4 peripheral slots and contains a backplane that provides a peak system throughput of 533 Mbytes/sec. An alternate unit using a peak bandwidth of 264 MB/s and allowing 6 peripheral slots is also supported.

To allow maximum flexibility, the electrical fibre channel interface between boxes was optimized for distances of 1 to 100 ft. An optional optical fibre channel interface will allow greater distances.

Time correlation is of utmost concern when distributed multiplexer architecture and/or multiple storage media are used. Each box receives IRIG time. Additionally, each box maintains a Relative Time Counter in accordance with IRIG-106 Chapter 10. So equipped, each device generates time packets conforming to Chapter 10 Time Data Packets. Time Data Packets are generated at 1-second intervals and transmitted to the master multiplexer for recording. To accommodate simultaneous recording sessions, the master broadcasts all Time Data Packets to all active recording sessions. Thus, in a

multi-box system, multiple data channels exist for time; one per box, and each time channel is broadcast to all active recording sessions.

The units packetize all ingress port data in accordance with the Chapter 10 standard. Each packet contains the Packet Header. Within the Packet Header, the Relative Time Counter value represents the free-running counter maintained on the box from which the original ingress port data was captured. The units support packet types that require Intra-Packet Time Stamps as per Chapter 10. All Intra-Packet Time Stamps containing relative time (as indicated by the Packet Flags in the Packet Header) shall conform to the same requirement as Relative Time Counter values. Thus, Intra-Packet Time Stamp values represent the free-running counter maintained on the box from which the original ingress port data was captured. In accordance with Chapter 10, for a given recording session, multiplexer units (master or slave) do not store ingress port data until a representative Time Data Packet for the original ingress port's box has been recorded.

All data packetized in accordance with IRIG-106 Chapter 10 must include a 16-bit unique value to all channels called channel ID. To allow a unique channel ID in a distributed multiplexer system, Teletronics has enhanced the semantics for Packet Channel IDs. The enhanced Channel ID uniquely identifies the original location of a packet's ingress into the system. Teletronics Channel IDs maintain Chapter 10 compliance, while defining sub-fields for box, slot, port, and logical channel ID as shown below.

msb															lsb
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Box			Slot				Port			Logical Channel ID					

Box: This 3-bit field represents a physical box address in a multi-box solution. Box addresses range from 0 to 7, with a master multiplexer (the unit that interfaces with the recording media) typically assigned address 0.

Slot: This 4-bit field represents a physical slot within a given box unit. Slot numbers range from 0 to 15, typically with the unit's processor board occupying slot 0, and slot numbers increasing with distance from the processor.

Port: This 3-bit field represents a physical port within a board. Port numbers range from 0 to 7. The relationship between port numbers and the physical location of external connectors is board-specific.

Logical Channel ID: This 6-bit field represents a logical channel ID within a port's data stream. Logical channel IDs range from 0 to 63. The logical channel ID is "0" for all port types that do not define logical channels.

As a result of the channel ID breakdown, all channels from a system utilizing a single multiplexer box or from a master multiplexer in a multiple box system will have channel

IDs ranging from 0x0001 through 0x0FFF. All channels from slave multiplexer box 1 in a multiple box system will have channel IDs from 0x1001 through 0x1FFF, and so on. Time data packets in a multiple box system will have a unique channel IDs.

Conclusion

The distributed system architecture discussed here allows for the creation of flexible multiplexer / recorder system that can accommodate from a few channels to a large amount of channels, and allows over 100 me gabytes per second of data acquisition, multiplexing, health monitoring, recording and general-purpose airborne processing in a modular, yet compact package rugged enough for the avionics environment.

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