

THE USE OF AN IRIG-106 CHAPTER 10 RECORDER AS A TELEMETRY SYSTEM

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ABSTRACT

IRIG-106 Chapter 10 has become the recording standard for most of the new flight test programs and many of the current ongoing programs. The primary goal of the standard was to define a common format for recording 100% bulk data such as PCM, MIL-STD-1553 busses, Video/Audio, ARINC-429, Ethernet, IEEE-1394, Analog Data, and others. In most cases the standard has provided the instrumentation engineers and the data analysts with a recording solution that meets their needs. Many programs require transmission of safety of flight data from a subset of the data acquired by the recorder. This may include selected video/audio channels, selected avionics bus data, and others. This requirement presents a dilemma to the flight test engineer who must duplicate part of the system for telemetry.

This paper discusses several applications in which the IRIG-106 Chapter 10 recorder can be used as a telemetry system. It will include the transmission of bulk MIL-STD-1553 data per IRIG-106 Chapter 8, transmission of multiple Video/Audio and PCM data channels, and transmission of selected avionics data per IRIG-106 Chapter 4.

KEY WORDS

Recorder, IRIG-106 Chapter 10, IRIG-106 Chapter 8, IRIG-106 Chapter 4, Video, MIL-STD-1553

INTRODUCTION

IRIG-106 Chapter 10 defines an “operating system-independent” file structure and packet format of several data types for recording. These packet formats define each data type structure for 100% data recording. Chapter 10 became the standard for bulk data recording, and has been adapted by most programs in the flight test community, as well as for some mission recording applications. As a recording standard, Chapter 10 achieved its primary goal to standardize on a recording format. Real world applications demand that the Chapter 10 Multiplexer / Recorder include additional functionality to telemeter data derived from the data source to be recorded. The TM data may include 100% data from several MIL-STD-1553 busses per IRIG-106 Chapter 8, Video / Audio and PCM data per IRIG-106 Chapter 4 Class II PCM, or selected avionics bus data from IRIG-106 Chapter 4 Class I PCM. Allowing TM capability from within the Chapter 10 Multiplexer / Recorder minimizes the need to duplicate the acquisition of the same data sources

being recorded. The TM capability can either be a built-in function or one that users can add using plug-in cards.

This paper will describe a Multiplexer / Recorder architecture that enables the use of TM data, and then discusses three applications where TM was required from within the Chapter 10 Multiplexer / Recorder to save cost and space (size) while maintaining the data recording format specified by IRIG-106 Chapter 10.

Multiplexer / Recorder Architecture

The basic architecture consists of a multi-slot custom cPCI chassis populated with a common set of system and I/O peripheral cards with either built-in recording media or external media. The baseline unit supports a total of 4 peripheral slots and contains a backplane that provides a peak system throughput of 533 Mbytes/sec. An alternate chassis using a backplane that provides a peak bandwidth of 264 Mbytes/sec and providing 6 peripheral slots is also supported. All peripheral cards are interchangeable between different chassis sizes and allow the user to configure a unit to support a large variety of different interfaces and port count per interface. The PowerPC processor is contained on the overhead card along with 256 megabytes of high-speed SDRAM and 32 megabytes of non-volatile storage. Two RS-232/422 configurable serial ports are supported along with eight general-purpose input/output signals. Figure 1 shows the relationship between the overhead card, system backplane and peripheral cards within a single unit. The PowerPC processor provides a centralized function where system configuration and management are performed, and acts as a traffic cop in scheduling the movement of data between peripheral cards in the unit. Central to the performance of the unit is the use of a 16.8 gigabit per second memory bus that allows for peak data throughput within the system.

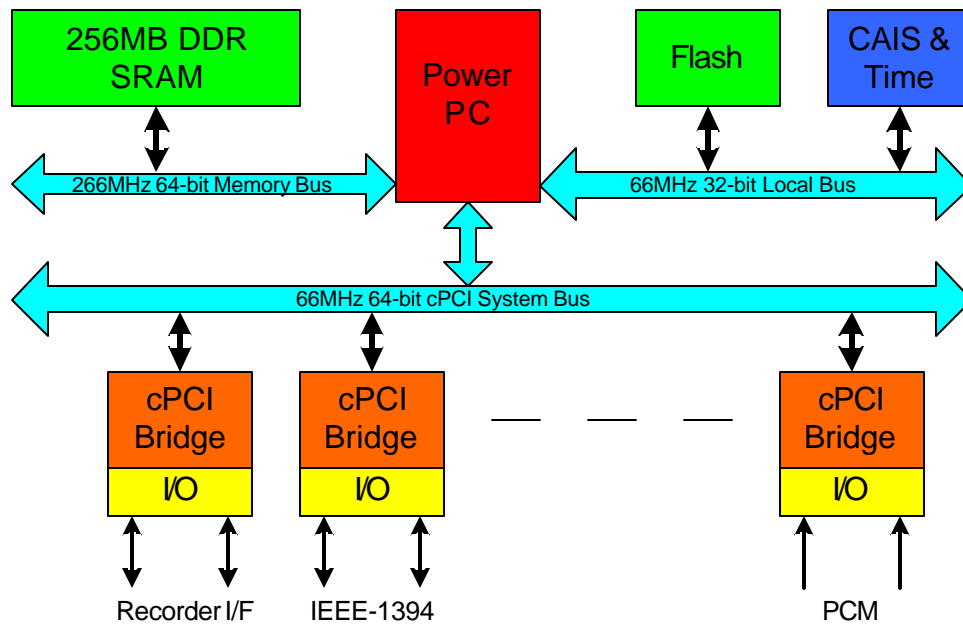


Figure 1. Multiplexer Architecture

The system backplane makes use of a 66 MHz, 64-bit backplane to move data between cards. The backplane is transparently compatible with both the PCI 2.2 specification and the PCI-X 1.0 specification, allowing an incremental path for the user in the future to achieve backplane speeds approaching 8 gigabits per second. Each peripheral card contains either a PCI 2.2 or PCI-X 1.0 compatible bridge to interface with the system backplane, depending upon the bandwidth requirements. The supported peripheral cards acquire data from Fibre Channel (electrical and optical), IEEE-1394B, PCM, MIL-STD-1553, ARINC-429, FOTR, Ethernet (BaseT and BaseFX), Video / Audio, Analog, Discrete, and other user specific cards.

Application 1: TM of MIL-STD-1553 Per IRIG-106 Chapter 8

Most IRIG-106 Chapter 10 recorders have the capability to acquire MIL-STD-1553 bus data for recording. The packet recording format and the data time stamp of the 1553 messages are straightforward and well defined in the Chapter 10 standard. A user generally requires to TM all MIL-STD-1553 buses or selected buses per Chapter 8 while recording all the data per Chapter 10. The simple solution is to duplicate the acquisition of the 1553 buses using a separate unit, and then TM that data. This solution is costly, requires additional bus couplers, additional aircraft wiring, and space for the additional acquisition unit. The better solution is for the Chapter 10 recorder unit to provide IRIG-106 Chapter 8 TM data from the acquired 1553 buses. This can be done either by the 1553 acquisition peripheral card or by an additional peripheral card in the unit. In this case, the solution was to realize the TM function as part of the peripheral I/O card as shown in figure 2.

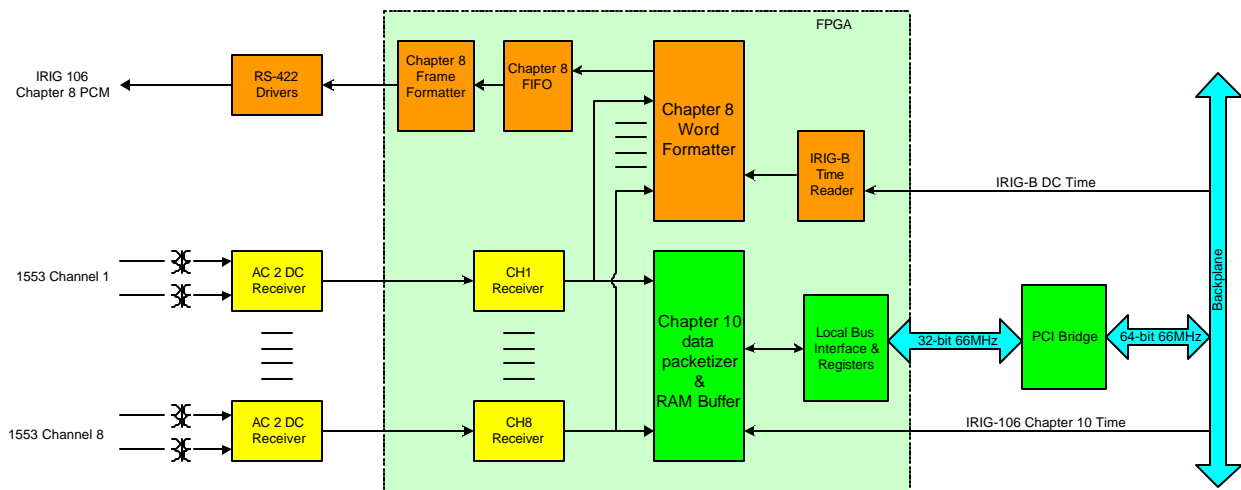


Figure 2. Architecture of an 8 channel 1553 card with IRIG-106 Chapter 8 PCM output

Acquired MIL-STD-1553 bus data is routed through two different data paths within the FPGA:

- IRIG-106 Chapter 10 Path
- IRIG-106 Chapter 8 Path

The Chapter 10 path circuitry time stamps the incoming data per the Chapter 10 standard (a 48-bit relative host chassis time with 100 ns resolution) and packetizes the data messages to be transported over the backplane to the host chassis's processor for data recording.

The Chapter 8 path circuitry time stamps the incoming data with absolute time derived from the IRIG time bus, adds the bus ID (one of eight buses) and data label per Chapter 8, and writes that data into a composite FIFO. The Chapter 8 formatter reads the FIFO at a programmable word rate defined during system configuration. The Chapter 8 PCM output operates at up to 12 Mbps, 24-BPW, and 128 or 256 words per frame.

Application 2: TM Selected Data Parameters per IRIG-06 Chapter 4 Class I PCM

The multiplexer / Recorder system described here and in [1] [2] provides the user with the capability to configure the chapter 10 recorder as a CAIS (Common Airborne Instrumentation System) DAU (Data Acquisition Unit) for the purpose of retrieving selected data parameters by a CAIS controller over the CAIS bus. In some cases this capability is not possible due to the selected data bandwidth of greater than the 5 Mbps limitation of the CAIS Bus, or the need to use the recorder only without a CAIS controller. The need to select specific data parameters for TM within the Chapter 10 recorder is rather obvious. The capability to “cherry pick” data parameters from Fibre Channel buses, IEEE-1394 buses, MIL-STD-1553 buses, FOTR buses and others enables the recorder to be used as a standalone data acquisition unit without the duplication of hardware. This powerful capability (shown in figure 3) enhances the functionality of the recorder well beyond the simple task to record data as defined in the IRIG-106 Chapter 10 standard.

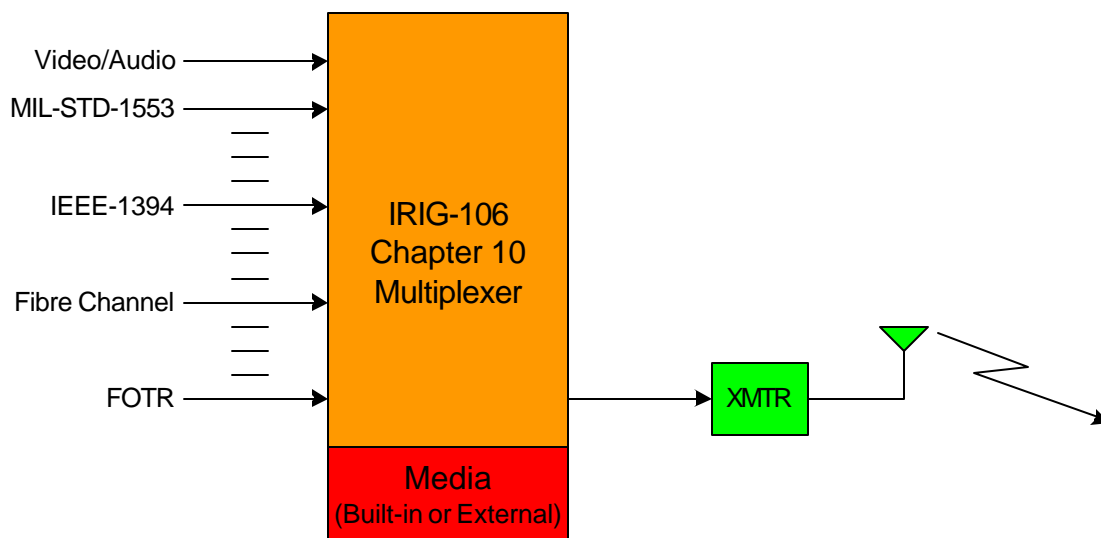


Figure 3. Chapter 10 Recorder as Data Acquisition / TM System

The functionality to TM selected data parameters is realized within a peripheral I/O card that receives its format map and data over the PCI bus from the unit’s overhead processor. The card utilizes a PCI bridge device, an FPGA, a 128K x 32-bit Dual Port RAM data memory, a 128K x 16-bit device organized as 64K x 32-bit as a format memory, a CVSD voice input, a digitally controlled 6 pole Bessel premod filter and a Direct Digital Synthesizer (DDS) to provide programmable PCM rate up to 20 Mbps in steps of 1 Hz.

The user defines the desired parameters to be selected as part of the configuration of the peripheral I/O card receiving that parameter, and defines the sampling rate and sampling position of that parameter as part of the format map when configuring the TM peripheral card.

Application 3: TM Multiple Video/Audio and PCM data

Most instrumentation aircraft use a video telemetry system in parallel to data acquisition and recording systems. In addition, the recording system acquires the same video/audio channels being transmitted for recording purpose. The requirement to acquire video / audio once by the chapter 10 recorder for both recording and real time transmission eliminates hardware duplication and reduces cost. In some applications the video data is already compressed over the aircraft Fibre Channel to be recorded - in this case the conventional video transmission will not work and would require a different method of data acquisition and transmission. This is in fact the case for the JSF (F-35) program. Additional requirements include the transmission of multiple video/audio and PCM channels from within the Chapter 10 recorder, and real time hardware-based data reconstruction of the video/audio and PCM channels as shown in figure 4.

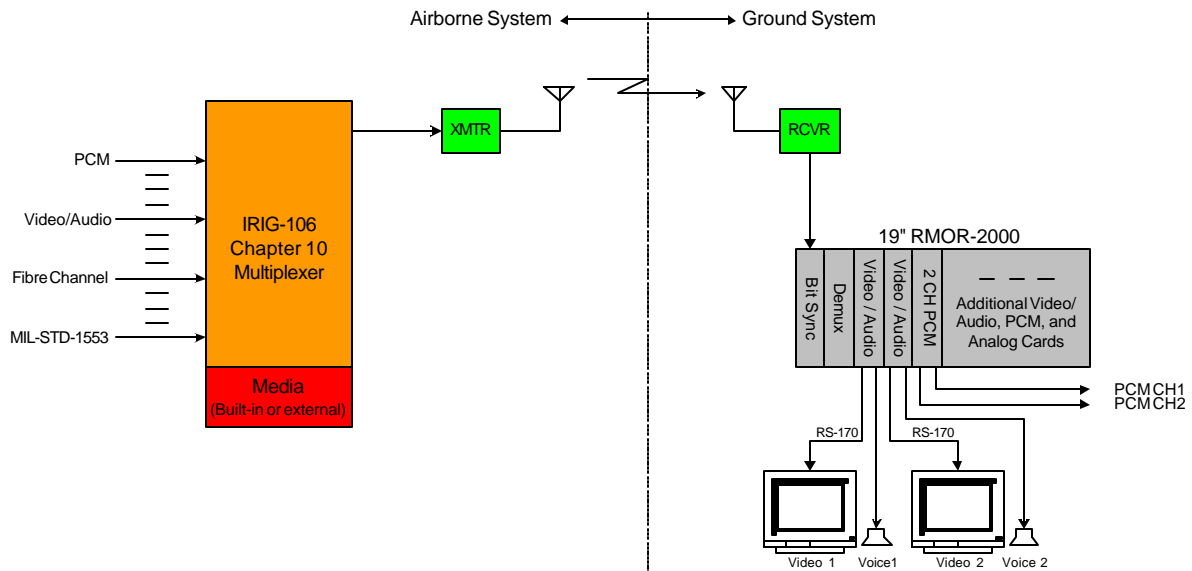


Figure 4. Chapter 10 Recorder with real time Video / Audio and PCM Transmission

The functionality to TM 100% data of selected video / audio and PCM channels is realized within the same peripheral card used to acquire selected data parameters, simply by using a different FPGA load. The card utilizes a PCI bridge device, an FPGA, a 128K x 32-bit Dual Port RAM data memory configured as 16 FIFOs for up to 16 channels, a 128K x 16-bit device organized as 64K x 32-bit as a format memory, a CVSD voice input, a digitally controlled 6 pole Bessel premod filter and a Direct Digital Synthesizer (DDS) to provide programmable PCM rate up to 20 Mbps in steps of 1 Hz.

The overhead processor is responsible for recording all incoming data per IRIG-106 Chapter 10. The processor is also responsible for sending data from selected channels to be transmitted to the designated channel FIFO on the TM card. Data is retrieved from each channel's FIFO at a preprogrammed sample rate for transmission. The format is generated based on an algorithm that only considers the data rate of each channel and the relative rates among the transmitted channels. The transmission rate is calculated as the sum of the rates of all channels to be transmitted plus 12% to 15%. The data format is fixed at 500 words per frame and 16 BPW. Every channel is allocated a block of words in the format based on its relative rate to other channels and the number of channels to be transmitted. Each word includes a flag bit to indicate if the data word is valid and to guarantee a bit transition every 16th bit at a minimum. For the algorithm to operate properly, all transmitted data channels must provide data at a predictable, constant data rate. In the case of video/audio channels, they must be configured at a constant rate and not at a variable rate.

The ground-based Rack Mount Output Reproducer (RMOR) unit is programmed with the same airborne format and additional information to map airborne acquisition channels to ground output channels. Each output channel uses a Direct Digital Synthesizer that is controlled by the channel processor to regenerate the exact data rate of the acquired airborne channel. A variation of up to +/- 6% in the rate of the airborne channel will result in a tracking rate change in the output channel with no change in the transmission rate. Any rate change greater than 6% in the input channel may result in lost data due to FIFO overflow.

The Chapter 10 recorder can be preprogrammed with up to 8 TM formats that can be invoked by the pilot using three discrete signal inputs. The formats are used to transmit different video/audio and PCM channels for different test points without affecting the recording process. The selected format is transmitted together with the data to allow the ground-based RMOR to invoke the proper settings based on the received format. The important element to this capability is that the transmitted data rate shall not change when format is changed. To do so, all formats are programmed to operate at the highest data rate format of up to 20 Mbps.

Conclusions

It was shown that the IRIG-106 Chapter 10 recorder can operate as a data acquisition unit and as a data and video telemetry unit without sacrificing the recording process. This approach allows the instrumentation engineers to save cost, wiring and space by using the Chapter 10 recorder as a telemetry system.

REFERENCES

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